Amendments to the Drawings:

The attached sheets of drawings replace the original sheets which include Figs. 1-3.

Attachment: Replacement Sheets
Annotated Sheet Showing Changes

REMARKS/ARGUMENTS

Claims 1-13 were pending. The drawings are objected to because they fail to show "the arbiter 100" as described in the specification on page 6 line 23. Upon entry of this amendment amending claims 1, 6, and 11, and adding claims 14-20, claims 1-20 remain pending.

Claims 1-3 stand rejected under 35 U.S.C § 112, first paragraph. Claims 1-13 stand rejected under 35 U.S.C § 102 and 35 U.S.C § 103 as being anticipated by ARM PrimeCell™ Multiport Memory Controller (PL176) revision r0p1, Technical Reference Manual", June 2003) (hereinafter "ARM").

Applicants aver that no new matter has been added in this response.

Interview with Examiner

Applicants appreciate the interview with the Examiner on May 15, 2006, where claim amendments and the cited prior art were generally discussed.

Drawing Objections

In the Office Action, the Examiner objected to the drawings not showing the term "the arbiter 100". Applicants have amended the specification accordingly, and believe that the objection is now moot.

§ 112 Rejection

In the Office Action, the Examiner rejected claims 1-13 under 35 U.S.C § 112, first paragraph. Applicants submit that the specification is written in full clear and concise terms to enable one skilled in the are to make and use the subject matter as claimed, at least as disclosed in pages 4-7 and Figure 3 of the specification as filed, and therefore submit therefore that the rejection of claims 1-13 is moot.

§ 102/103 Rejections

Claims 1, 6, and 11

In the Office Action, the Examiner rejected claims 1-13 under 35 U.S.C § 102 as being anticipated by ARM and 35 U.S.C § 103 as being obvious in view of ARM. The Examiner stated that per claim 1, 6, and 11 ARM discloses multiple bus interfaces each capable of receiving memory access requests for read access which may exceed the burst access length of the memory accessed by the controller, and the means to queue such requests where multiple corresponding memory transactions may result in satisfaction of a read access request such that back-to-back SDRAM read burst may be performed citing chapter 1 and chapter 2 *et seq.* of ARM. Applicants respectfully traverse the rejections.

ARM does not disclose all of the elements of amended claims 1, 6, and 11, and therefore the claims are patentably distinguished over the reference. For example, claim 1 partially recites, "control logic *calculates the number of required data bursts and a starting address for each burst, and places the respective memory access requests into the queue* of memory access requests such that back-to-back SDRAM read bursts can be performed...wherein *the control logic determines whether the read access request is for data that can be delivered in a single burst of data, or for data that requires multiple bursts of data*", claim 6, recites in part "*determining from a memory access request if the memory access request requires a single burst of data, or multiple bursts of data* to be read from the memory device...when a memory access request is a read access request which requires multiple bursts of data to be read from the memory device, calculating the number of required data bursts", and claim 11 recites in part "control logic, for receiving memory access requests from the or each first bus interface, for *calculating a required number of data bursts needed to deal with each received memory access request*, and for *determining if the memory access requests require a single data burst or multiple data bursts*" (emphasis added).

ARM merely discloses that "All Burst types are supported" on page 2-29 of ARM and on page 2-4 discloses a command sequencer that holds up to 10 requests which are prioritized and rearranged to maximize memory bandwidth and minimize transaction latency. At the time the claimed subject matter was filed, ARM merely listed the features of the memory

controller and was silent to calculating the number of burst required and was also silent to the determination by the logic circuit if the data request can be serviced using a single burst of data, or requires multiple bursts of data, as claimed. Therefore, Applicants submit that claims 1, 6, and 11 are patentably distinguished over the cited reference, alone or in combination.

Claims 2-5, 7-10, 12-13

Claims 2-5 depend from claim 1, and claims 7-10 depend from claim 6, and claims 12-13 depend from claim 11 and are therefore allowable for at least the reasons discussed in relation to claims 1, 6, and 11, as well as the limitations they recite.

Added Claims

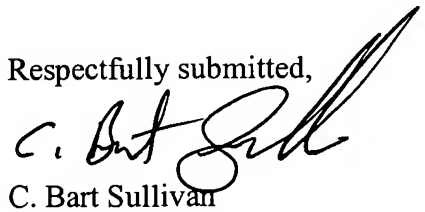
New claims 14-20 are supported at least in Figures 1-3 and on page 2, lines 1-22, page 4, lines 1-30, page 5, lines 5-30, and page 6, lines 5-35 in the specification as filed.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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Attachments
CBS:rgy
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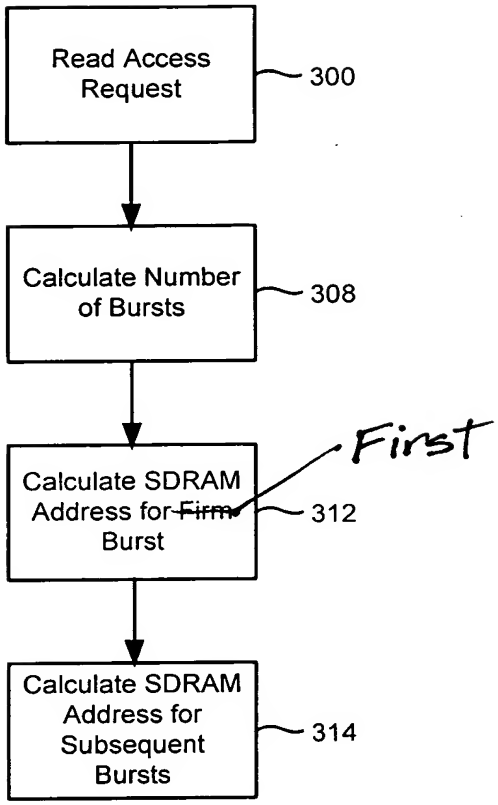
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Calculate Number of Bursts
308
First
Calculate SDRAM Address for ~~Firm~~ Burst
312
Calculate SDRAM Address for Subsequent Bursts
314

Fig. 3